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 Apr 2003  
 ...leading edge, the **simulation** model would be incorrect...illegal Verilog RTL **synthesis** coding style) the **simulation** model would not be correct for a **flip-flop** and Synopsys would...reading the model for **synthesis**. For VHDL, including...  
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 ...Describing the Design 52 4.4 **Synthesis** of Digital Logic 62 4.5...Verification and Validation 139 7.2 **Simulation** 141 7.3 Additional Considerations for **Simulation** 144 7.4 Application Specific...for Positive Edge Clocked **Flip-Flop** 34 v 22 Synchronization...Coding Example 61 32 Logic **Synthesis** Process 64 33a Hierarchical...  
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 Nov 2004  
 ...and then **simulation** B. **simulation**, then FPGA place & route, and then **synthesis** C. **simulation**, then **synthesis**, and then FPGA place & route...Signal C. Both of them 7) A D **flip-flop** output can become **metastable** when: A. the clock is too...  
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- ☐ 4. [Ian G. Clark - Metastability Bibliography](#) [94K]  
 Sep 2004  
 ...Synchronizers Operating in **Metastable** Region", IEEE Transactions...Dynamics of Bistable **Flip-Flops**", 6th Int. Symp...Davies,

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### Simulation and Synthesis Techniques for Asynchronous FIFO Design with Asynchronous Pointer ...

CE Cummings, P Alfke - SNUG 2002 (Synopsys Users Group Conference, San Jose, CA, ..., 2002 - sunburst-design.com

... **Simulation and Synthesis** Techniques for ... The first **flip-flop** could go **metastable**, which is why there is a second **flip-flop** in the dual synchronizer. ...

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### SAME 2004

S Bernardi, S Lebailly, T Instruments, B Blanc, G ... - signal - same-conference.org

... top-level is valid for **simulation** and verification ... reduction of compilation and **synthesis** time • Better ... or hold time; thus, causing a **metastable** condition and ...

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### Using hierarchical clock tree **synthesis** to generate balanced clock trees

P Ragon, A Dugar - Integr. Syst. Des, 1997 - eedesign.com

... cause **flip-flops** to operate in **metastable** states and ... However, because **simulation** requires developing test vectors, we ... The ASIC **synthesis** tool we had chosen had ...

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### Synchronous Resets? Asynchronous Resets? I am so confused! How will I ever know which to use?

CE Cummings, D Mills - SNUG 2002 (Synopsys Users Group Conference, San Jose, CA, ..., 2002 - sunburst-design.com

... add any **synthesis** attributes to get the **synthesis** tool to ... is not part of cycle based **simulation**, the asynchronous ... of the **flip-flop** could go **metastable** and thus ...

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### Communication Between Independent On-Chip Synchronous Systems

I Brynjolfson - macs.ece.mcgill.ca

... N. Vijaykrishnan, "Energy Efficient Datapath **Synthesis** Using Dynamic ... and R. Brodersen, "The **Simulation** and Evaluation ... to obtain a **metastable** response from ...

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### A METHOD FOR HIGH RELIABILITY FIELD PROGRAMMABLE GATE ARRAY (FPGA) DESIGNS

D Albaiges, FE Branch - klabs.org

... Does timing **simulation** meet functional and performance requirements? Return to DESIGN, **SYNTHESIS**, or PLACE & ... result in **metastable** conditions at the synchronizer ...

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### Verifying Synchronization in Multi-Clock Domain SoC

T Kapschitz, R Ginosar, R Newton - 2004 - athdl.com

... timing violations may cause signals to go **metastable**; they also ... [www.athdl.com/products.html](#) [5] Cliff Cummings, "**Simulation and Synthesis** Techniques for ...

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CÉ Cummings - Synopsys Users Group Conference, San Jose, CA, [www. sunburst ...](http://www.sunburst.com), 2001 - [vlsidsp.el.yuntech.edu.tw](mailto:vlsidsp.el.yuntech.edu.tw)

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... add any **synthesis** attributes to get the **synthesis** tool to ... is not part of cycle based **simulation**, the asynchronous ... of the **flip-flop** could go **metastable** and thus ...

... manner similar to edge-triggered D **flip-flop**, but with ... Studies of the **metastable** condition rele- vant to this ... 7. DL-DFLOP NOR sequence recognition **simulation**. ...

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Expert Verilog, SystemVerilog & **Synthesis** Training. **Simulation** and **Synthesis** ...  
avoid **metastable** problems as described below). This is not a problem. ...

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some of the hardware design, timing analysis, **synthesis** and **simulation** ...  
Synchronization failure is caused by an output going **metastable** and not ...

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cific problem is to avoid **metastable** states which might drive the FSMs into unknown  
... [1] Clifford E. Cummings, Peter Alfke, **Simulation** and **Synthesis** ...

[mufasa.informatik.uni-mannheim.de/Lectures/SS05/HWE/script/fifos.pdf](http://mufasa.informatik.uni-mannheim.de/Lectures/SS05/HWE/script/fifos.pdf) - [Similar pages](#)

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designers to add synchronizers to reduce the probability of **metastable** signals  
... automatically finds common RTL errors, **simulation-to-synthesis** mismatch ...

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Crystallization" deal with the **synthesis** of **metastable** amorphous and crystalli-  
... Using **simulation** techniques the structure of these materials could be ...

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Unfortunately the influence of **metastable** phases, kinetic effects and non-equilibrium  
conditions, ... tion and improved **synthesis** methods provide greater ...

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**simulation** of materials **synthesis**, processing, micro- ... **Metastable** and inhomogenous  
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Development of improved constitutive models and **simulation** capability for processing !  
... Title: "**Synthesis** of **Metastable** Carbon-Silicon Nitride by ...

